REMARKS

This paper is being provided in response to the Final Office Action dated September 20, 2005, for the above-referenced application. In this response, Applicant has made minor modifications to the specification and cancelled claims 13 and 18. Applicant respectfully submits that the amendments to the specification do not add new matter.

Applicant gratefully acknowledges the allowance of claims 2-12 and 15-17.

The objection to the specification has been addressed by amendments to the specification provided herein in accordance with the guidelines set forth in the Office Action. Accordingly, Applicant respectfully requests that this objection be withdrawn.

The rejection of claims 1, 13, 14 and 18-20 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,397,931 to Bayer (hereinafter "Bayer") is hereby traversed and reconsideration is respectfully requested. Claims 13 and 18 have been cancelled herein.

Independent claim 1 recites a boosting circuit including first, second and third charge pump circuits containing first, second and third capacitive sections all charged to a first voltage. A switching unit connects the first charge pump circuit, the second charge pump circuit and a first node in series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from the first node to a first internal circuit of a semiconductor device. The switching unit further connects the first charge pump circuit, the second charge pump circuit, the third charge pump circuit and a second node in series in

response to a second switch signal and the control signal, such that a third voltage is outputted from the second node to a second internal circuit of the semiconductor device.

Independent claim 14 recites a semiconductor device including a boosting circuit and first and second internal circuits connected to the boosting circuit via first and second nodes. The boosting circuit includes first, second and third charge pump circuits containing first, second and third capacitive sections all charged to a first voltage. A switching unit connects the first charge pump circuit, the second charge pump circuit and the first node in series in response to a first switch signal and a control signal such that a second voltage higher than said first voltage is outputted from the first node to the first internal circuit of a semiconductor device. The switching unit further connects the first charge pump circuit, the second charge pump circuit, the third charge pump circuit and the second node in series in response to a second switch signal and the control signal, such that a third voltage is outputted from the second node to the second internal circuit of the semiconductor device.

Independent claim 19 recites a method of boosting a voltage. First and second capacitors are charged to a first voltage in first and second modes. A potential of the first capacitor is boosted to twice that of the first voltage in said first and second modes. The first and second capacitors are connected in series in the first mode to output a second voltage. A third capacitor is charged to the first voltage in the second mode. The first, second and third capacitors are connected in series in the second mode to output a third voltage. The method includes switching between first and second modes in response to a control signal and first and second switch signals. Claim 20 depends from independent claim 19.

Bayer discloses a charge pump-type DC/DC converter that includes n elementary stages, each consisting of a charge pump capacitor and several controllable switches connected thereto, whereby the input voltage of the DC/DC converter is applied to the input of the first stage, both electrodes of the charge pump capacitor of the kth stage are each connectable to one of the controllable switches with the output of the (k-1)th stage, k=2, . . . , n and the output of the nth stage forms the output of the DC/DC converter. Each stage includes charge pump capacitor (CFly1, CFly2, ...) that is charged by the input applied to that stage to a voltage corresponding maximally roughly to the input voltage to that stage (see, for example, column 2, lines 48-53). Each stage also includes a storage capacitor (COUT1, COUT2, ...) provided at the output of each stage (see, for example, column 2, lines 59-65). As set forth beginning at the bottom of column 2, the output of each stage is doubled from stage to stage.

Applicant's independent claims 1, 14, and 19 all recite multiple charge pump circuits (multiple stages) having a capacitive section (claims 1 and 14) or a capacitor (claim 19) charged to a first voltage. In contract, Bayer discloses doubling the voltage at each stage and thus, for Bayer, no two stages, and thus certainly no three stages, would arguably have capacitors or capacitive sections charged to the same voltage (a first voltage), a feature recited in Applicant's claims 1, 14, and 19. The Bayer device provides a 2^k voltage gain where k is the number of stages. This is in direct contrast to the features recited in Applicant's claims 1, 14, and 19 where each stage has a capacitive or a capacitor charged to a first voltage (i.e., the same voltage). Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 508-898-8603.

Respectfully submitted,
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